REMARKS

Applicants respectfully request that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicants submit that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicants believe that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

No claims have been amended. No claims have been cancelled. Therefore, claims 1, 2, 6, 12-16 and 21-32 are now presented for examination.

Claims 1, 2, 6, 12-16, 21 and 24-32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kamiya (U.S. Patent No. 5,809,335) in further view of the applicant admitted prior art (AAPA). Applicants submit that the present claims are patentable over Kamiya in view of the AAPA.

Kamiya discloses a method and a data transfer apparatus capable of handling DMA block transfer interruptions. See Kamiya at Abstract. When a command for a DMA transfer through a certain DMA channel (e.g., CHn) is issued from a CPU, a DMA transfer-executing section first sets DMA control parameters stored in the DMA channel CHn. Next, the section selects the data buses corresponding to source and destination addresses (SA and DA), and data is DMA-transferred from an external module to another external module through the selected buses. Subsequently, the source address SA and the destination address DA are incremented, and the number N of data items to be transferred is decremented. Then, the DMA transfer-executing section determines whether or not the number N of data items to be transferred is equal to 0. If the number N of data items to be transferred is equal to 0, the DMA block transfer is terminated. However, if the number N of data items to be transferred is not equal to 0, the transfer continues. See Kamiya at col. 4, ll. 22 - 55.

When a command for DMA transfer through a DMA channel CHn+1 higher in priority than the DMA channel CHn is issued during the DMA transfer through the DMA channel CHn, the source address SA, the destination address DA, and the number N of data items to be transferred are transferred to a backup channel information memory and saved into a backup channel BUPCHn corresponding to the DMA channel CHn. Next, a DMA transfer through the channel CHn+1 is carried out according to the routine described above. When the DMA block transfer is restarted based on the DMA control parameters saved in the backup channel BUPCHn, the information saved in the backup channel BUPCHn is set to the DMA transfer-executing section to restart the DMA transfer (col. 4, ll. 56 - col. 5, ll. 6).

The AAPA rejection is based upon applicants' background section in the specification. The background section discloses an I/O device coupled to a DMA channel. See Specification at Fig. 4A and page 2, line 13 - page 3, line 8. Nevertheless, neither Kamiya nor applicants' background section disclose or suggest a DMA controller that terminates a DMA transfer before a terminal count is reached upon receiving a retransmit request signal from the I/O device, or a DMA controller that re-executes a DMA transfer with an I/O device upon receiving a request from the I/O device.

Claim 1 of the present application recites:

> A system comprising:
> a direct memory access (DMA) controller; and
> an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device.

Applicants submit that neither Kamiya, nor the AAPA disclose or suggest receiving an early termination request signal from an I/O device. Moreover, neither reference discloses or suggests a DMA controller that terminates a DMA

transfer before a terminal count is reached. However the Examiner asserts that:

> It is quite clear from the reference that the transfer is terminated, and that only after an entirely different second DMA transfer is completed that the first transfer is restarted.

See Final Office Action at page 2, paragraph 1.

The Examiner's assertion affirms applicants' argument that Kamiya does not disclose or suggest a DMA controller that terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device. Kamiya discloses interrupting a first DMA transfer to execute a second DMA transfer having a higher priority. The second DMA transfer is executed. After completion of the second DMA transfer, the first DMA block transfer is resumed based on saved values. Applicants submit that the interruption and resumption of a DMA transfer is not equivalent to the termination of a DMA transfer.

Since neither Kamiya nor the AAPA disclose or suggest a DMA controller that terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device, any combination of Kamiya and the AAPA would also not disclose or suggest such a feature. Accordingly, claim 1 is patentable over Kamiya in view of the AAPA.

Claims 2 and 24-28 depend from claim 1 and include additional features. Therefore, claims 2 and 24-28 are also patentable over Kamiya in view of the AAPA.

Claim 12 recites:

> A system comprising:
> a direct memory access (DMA) controller; and
> an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller re-executes a DMA transfer with the I/O device upon receiving a retransmit request signal from the I/O device.

Applicants submit that neither Kamiya, nor the APA disclose or suggest receiving a retransmit request signal from an I/O device. Further, neither reference discloses or suggests a DMA controller that re-executes a DMA transfer. As discussed above Kamiya discloses resuming a first DMA transfer after the first DMA transfer has been interrupted to execute a second DMA transfer having a higher priority. Applicants submit that resuming an interrupted DMA transfer is not equivalent to re-executing a DMA transfer.

Since neither Kamiya nor the AAPA disclose or suggest a DMA controller that re-executes a DMA transfer with an I/O device upon receiving a retransmit request signal from the I/O device, any combination of Kamiya and the AAPA would also not disclose or suggest such a feature. Consequently, claim 12 is patentable over Kamiya in view of the AAPA. Because claims 29-32 depend from claim 12 and include additional features, claims 29-32 are also patentable over Kamiya in view of the AAPA.

Claim 13 recites:

> A method comprising:
> transferring data between a first device and a second device under control of a direct memory access (DMA) controller;
> receiving a request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;
> transmitting an acknowledge signal from the DMA controller to the first device; and
> re-transferring the data between the first device and the second device.

For the reasons described above with respect to claim 12, claim 13 is also patentable over Kamiya in view of the AAPA. Since claim 14 depends from claim 13 and includes additional limitations, claim 14 is also patentable over Kamiya in view of the AAPA.

Claim 15 recites:

> A method comprising:

transferring data between a first device and a second device under control of a direct memory access (DMA) controller;

receiving a request signal at the DMA controller from the first device indicating a request by the first device to terminate the transfer of data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

For the reasons described above with respect to claim 1, claim 15 is also patentable over Kamiya in view of the AAPA. Because claims 16, and 21-23 depend from claim 15 and include additional limitations, claims 16, and 21-23 are also patentable over Kamiya in view of the AAPA.

Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kamiya in further view of the applicant admitted prior art (AAPA) as applied to claims 1, 2, 6, 12-16, 21 and 24-32 above, and further in view of Murray (U.S. Patent No. 5,903,775).

Applicants submit that the present claims are patentable over any combination of Kamiya, the AAPA and Murray.

Murray discloses a method for allowing the transmission of digital video segments along a number of transmission channels. See Murray at Abstract. Nevertheless, Murray does not disclose or suggest a DMA controller that terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from an I/O device. In addition, Murray does not disclose or suggest a DMA controller that re-executes a data transfer upon receiving a request from an I/O device.

As previously discussed, Kamiya and the AAPA do not disclose or suggest the above features. Therefore, any combination of Kamiya, the AAPA and Murray also would not disclose or suggest a DMA controller that terminates a DMA

transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device, or a DMA controller that re-executes a data transfer upon receiving a request from an I/O device. Accordingly, the present claims are patentable over Kamiya in view of the APA and further in view of Murray.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request that the rejections be withdrawn and the claims be allowed.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on July 9, 2004.

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Name

Signature